IN THE SPECIFICATION

Please amend the paragraph inserted in the Preliminary Amendment of December 8, 2003 before the paragraph beginning at page 1, line 3 as follows:

This application is a continuation of U.S. Patent Application Serial No. 09/489,130, now U.S. Patent No. [[_____]] 6,671,795.

Please amend the paragraph beginning at page 7, line 22 as follows:

According to another embodiment of the present invention, a pause instruction is implemented with a timer or counter. As shown in FIG. 3, the memory flag 19 of FIG. 1 is replaced by a counter 39. As a first example, when decode unit ~~21determines~~ 21 determines that the next instruction from a first thread is a pause instruction (i.e., an instruction having a particular bit format), then a predetermined value is loaded into counter 39. In this example, counter 39 counts down from the predetermined value to zero. While counter 39 counts down to zero, instructions from the second thread (e.g., thread 1) are decoded and loaded into the pipeline. In this example, decode unit 21 alternates between checking the value of counter 39 (instead of decoding instructions from thread 0) and decoding instructions from thread 1. Once the counter has finished (e.g., reached zero), the next instruction from that thread can be loaded into the pipeline. As a second example, the pause instruction will include an operand (i.e., a value to be loaded into the timer). Accordingly, this allows decode unit 21 to load the operand value into counter 39 so that the length of time for the pause instruction can be set.